High resolution inductively coupled plasma etching of 30 nm lines and spaces in tungsten and silicon

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(Received 1 June 2000; accepted 23 August 2000)

Dry etching of 30 nm features was investigated for x-ray and integrated electronics applications. These typically require etching of either a tungsten absorber layer or a silicon mold. Through the use of an inductively coupled plasma source and accurate control over substrate temperature it was possible to achieve highly anisotropic patterning of tungsten and silicon. Densely patterned features as small as 30 nm and at pitches of 70 nm were etched in tungsten and silicon, to depths of 100 and 200 nm, respectively. © *2000 American Vacuum Society.* [S0734-211X(00)18406-9]

I. INTRODUCTION

Patterning of sub-100 nm features has become essential for advanced research and development in electronics, optics, and material science applications. This is especially true for x-ray applications such as microscopy zone plate lenses.

The critical steps in the production of densely packed sub-100 nm features for x-ray applications are high resolution e-beam lithography and precisely controlled dry etching of x-ray absorber (tungsten) or mold (silicon or polymer) materials.

At the Lawrence Berkeley Nation Laboratory (LBNL) lithography is performed using the Nanowriter, an ultrahigh resolution 100 KeV, Gaussian, electron beam lithography system to expose electron-sensitive resist materials. Using the Nanowriter and a very high resolution e-beam resist, calix[1] arene (available from TCI America), we routinely pattern and electroplate sub 30 nm linewidth structures for x-ray applications such as microscopy zone plate lenses. However, we are near the limits of this technology. In order to push the envelope for these densely packed structures in terms of resolution, compromises in thickness have been made. Currently, the aspect ratio of the finest electroplated features is limited to around 1:1 by electron beam/substrate interactions in the resist. Because higher aspect ratio features would greatly improve device efficiency, dry etching is the critical key to improved performance for both additive and subtractive processes. In additive processing, dry etching transfers fine-feature patterns into a high aspect ratio tri-level ''mold,'' which is then filled in by electroplating metal into the mold. In subtractive processing, the high resolution pattern is etched directly into the substrate, using a high-selectivity hard mask.

In this article we describe the development of state-of-the-art inductively coupled plasma (ICP) dry etch processes for etching extremely fine and densely packed features in tungsten and silicon. Although small features have been etched previously, features this small with this fine packing has only been reported once previously (Ref. 2). Our work takes this process further by producing the densely packed fine features with better sidewalls and higher aspect ratios. This is critical for the production of the highest resolution x-ray optics.

The etching of these fine features requires advanced and sophisticated processes and equipment. The high ion density, low pressure ICP etch regime is one of the few ways to provide highly anisotropic profiles with excellent control over selectivity to mask materials. This article describes how we have combined high resolution electron beam patterning processes, ICP etching, low, well-controlled substrate temperatures, and new etch processes [that do not rely on polymer sidewall passivation Refs. 3, 4, and 5] to produce 30–35 nm gratings at dense (1:1) line-to-space ratios and high aspect ratios in tungsten and silicon.

In addition, all hard mask definition was carried out using dry etching, rather than metal lift-off, hence overcoming the inherent limitations of the lift-off technique, such as poor resolution (Refs. 4 and 6), inferior pattern edge quality, and low yield (particularly for grating patterns).

II. EXPERIMENTAL DETAILS

The system used for dry etching was a Plasmalab System 100 ICP etcher from Oxford Instruments Plasma Technology. A schematic of the etch chamber is given in Fig. 1. Oxford's ICP system was chosen for this investigation as it provides a high density plasma etch, giving highly anisotropic etch profiles and controllable selectivity to the masking materials.

Samples were loaded into the chamber via a loadlock to maintain good stability of chamber vacuum and hence excellent repeatability of etch results.

The 4 in. silicon wafers were mechanically clamped to a temperature-controlled electrode. Helium pressure was applied to the back of the wafers to provide good thermal contact between chuck and wafer.

The Plasmalab System 100 ICP has precise control of substrate temperature over a very wide temperature range ($-150\,^{\circ}\mathrm{C}$ to $+200\,^{\circ}\mathrm{C}$), through the use of electrical heater elements and a supply of liquid nitrogen. The wide tem-

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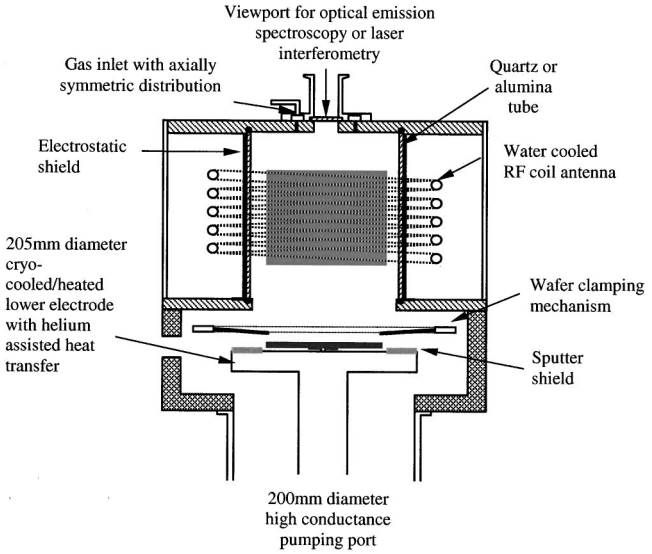

FIG. 1. ICP schematic.

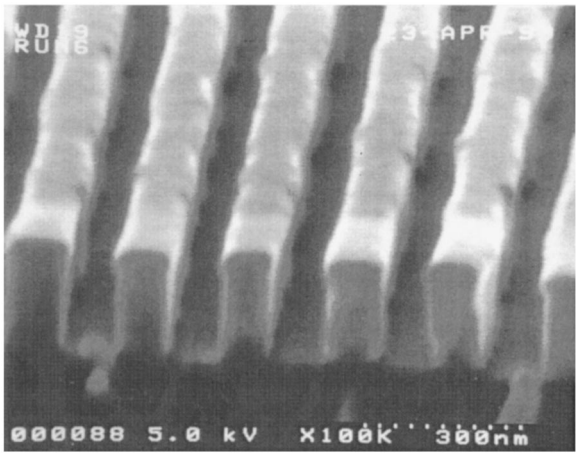

FIG. 2. Photoresist ICP etch using Ti mask (100 nm lines and spaces).

perature range is ideal for the development of advanced plasma etch processes for a wide variety of materials. Substrate temperature has a marked effect on the etch result, as it controls the volatility of the etch species and hence influences the chemical component of the process, affecting not only etch rate, selectivity, and profile, but also surface roughness.

Radio frequency power (13.56 MHz) is applied to both ICP source (up to 3000 W) and substrate electrode (up to 500 W) to generate the etch plasma. The electrostatic shield around the ICP tube is used to ensure that the ICP power is purely inductively coupled (i.e., ''true ICP''), hence eliminating sputtering of tube material and minimizing cross talk between rf generators. Ion energy at the substrate is monitored by measurement of the dc bias generated on the lower electrode, and is controlled mainly by the rf power supplied to this electrode.

It is also possible to operate this system in a purely reactive ion etching mode (RIE) mode, simply by applying power to only the lower electrode. This offers an extra degree of process flexibility as will be described in later sections.

The system can be operated over a pressure range from 0 to 100 mT allowing accurate control over operating pressure for both ICP mode and RIE mode processes.

Substrates were coated with 40 nm calix[1] arene and then patterned at LBNL using the Nanowriter, a modified Leica VB6-HR electron beam lithography system optimized for high resolution curvilinear shapes such as those used for x-ray zone plates. Details of the resist processing and patterning can be found elsewhere (Ref. 7).

A 40-nm-thick calixarene resist mask was used in all cases. The calixarene resist has a relatively high erosion rate during dry etching, so it was necessary to first transfer the high resolution patterns into an intermediate hard mask layer.

Two types of 4 in. hard mask/substrates systems were used for this investigation (1) 10 nm electron beam evaporated chrome on 100 nm sputtered tungsten on Si (100) and (2) 20 nm chemical vapor deposited low temperature silicon dioxide (LTO) on silicon (100). Substrate thicknesses were based on x-ray absorption criteria and hard mask thicknesses were based on chemical selectivity at the required substrate thicknesses as well as compatibility with other substrate systems.

Samples were baked at 110 °C for 30 min immediately before dry etch processing to improve the plasma etch resistance of the resist mask.

III. RESULTS: PRELIMINARY STUDY—A TRI-LEVEL PROCESS

The high resolution capabilities of the Plasmalab System 100 were initially investigated by dry etching the final layer of a tri-level process lithographic process. The top layer was lithographically defined using the Nanowriter and 100 nm of Shipley Sal 601 electron beam resist. The middle layer was 10 nm of e-beam evaporated titanium which was RIE etched by LBNL. The final layer was a UV hardened KRS photoresist (manufactured by IBM) which acts as a mold for electroplating. The pattern was transferred using an O_2 chemistry at low substrate temperature. Figure 2 shows a cross-sectional view of the resulting etched features. The Plasmalab System 100 clearly demonstrated the capability of etching sub-100 nm grating structures.

IV. LTO/SILICON ETCH RESULTS

Etching of the LTO was carried out using a CHF_3/Ar gas mixture in RIE mode (i.e., with no ICP power) to provide maximum selectivity to the calixarene resist. It has been found during previous etch evaluations that the selectivity to photoresist is reduced when operating with ICP power added. This is attributed to the excess formation of fluorine by the ICP source, leading to rapid resist erosion. LTO etching was carried out with the substrate temperature held at 20 °C.

TABLE I. Typical ICP parameters used during silicon and tungsten etch trials.

Total gas flow rate	30–60 sccm
Process pressure	5–10 mT
ICP power	250–750 W
DC bias	100–200 V
Temperature	See the text
Helium backing pressure	10–20 Torr

Through the use of an optimized RIE mode process an LTO etch rate of 400 Å/min and a selectivity (LTO:calixarene) of ~1.25:1 were achieved.

The silicon etching was performed using both the ICP and RIE power. A HBr process chemistry was chosen as it is known to be a highly anisotropic silicon etch with good selectivity to LTO. This process was operated with the substrate temperature held at 20 °C. Anisotropy is achieved due to the low volatility of the $SiBr_x$ etch product at this temperature, which forms a sidewall protective layer.

Typical ICP etch conditions are given in Table I. Selection of the correct operating parameters was determined by the need for adequate but not excessive etch rate, sufficient selectivity to mask materials, and optimum profile control. For example, at low ICP process pressures the selectivity to the LTO mask was too low, while at high pressures the etch rate and profile control were reduced. ICP power and dc bias were set to low-to-moderate levels to avoid heating of the samples, while gas flow rates were chosen to provide short gas residence times and hence a plentiful supply of etch species. The final optimized silicon etch process had an etch rate of 800 Å/min, with selectivity to the LTO hard mask of >10:1. Figure 3 shows a cross section of 50 nm lines etched 200 nm deep (4:1 aspect ratio) in silicon. Figure 4 shows a top view of 35 nm lines from the same wafer clearly defined.

The use of HBr in the silicon process has produced 200-nm-deep features in silicon with a vertical profile.

V. CHROME/TUNGSTEN ETCH RESULTS

The chromium etch process was developed using a Cl_2/O_2 chemistry. The process was optimized using test pieces taken from Cr-on-quartz photomask plates. The effects of chamber pressure, ICP power, RIE power, gas flows, and temperature on Cr etch rate and selectivity to resist were investigated. It was found that good transfer of the pattern from the resist to the underlying Cr film required an RIE-only process at low power and high pressure to minimize erosion of the calixarene resist. A low substrate temperature (−20 °C) was used to maintain good CD control. The final process had a Cr etch rate of 20 Å/min, with selectivity to calixarene of ~1:1.

Several tungsten dry etch methods have been reported previously. A common method is RIE using SF_6/CHF_3, typically in ratio 1:4 (Refs. 3 and 4), where the SF_6 is the etch gas and CHF_3 is added to form a polymer which protects the etch sidewalls to give profile control. However, this may have disadvantages, since CHF_3 will deposit polymer on the chamber walls, requiring frequent cleaning. The polymer in the chamber will in turn make the process more sensitive to chamber condition, hence reducing reliability of profile control. The polymer technique can also lead to excessive polymer deposited in narrow trenches compared to isolated features, leading to difficulty in etching narrow gratings (Ref. 5). We therefore chose to investigate a clean SF_6/O_2 based tungsten dry etch process, in which profile control is achieved through adjustment of O_2 content and substrate temperature.

The tungsten etch process utilized an SF_6 chemistry with both ICP and RIE power. The effects of substrate temperature (−20 to −50 °C) and O_2 addition on etched profile of sub-100 nm features were studied. Operating at low temperatures has been reported to improve tungsten etch anisotropy (Ref. 6) due to reduced volatility of the WF_x etch products. Addition of O_2 is also thought to be beneficial in this respect due to the formation of a less volatile WO_xF_y (Ref. 7). In both cases the low volatility of the WF_x and WO_xF_y improve anisotropy due to enhanced sidewall passivation.

Typical ICP etch conditions are given in Table I. During SF_6/O_2 etch optimization it was found that high ICP power

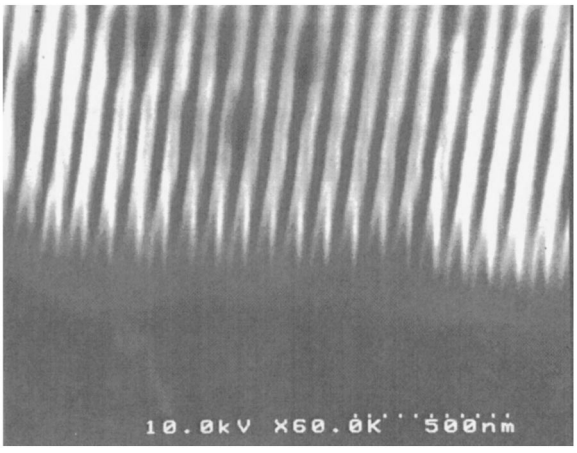

FIG. 3. Cross section of 50 nm lines and spaces etched into silicon.

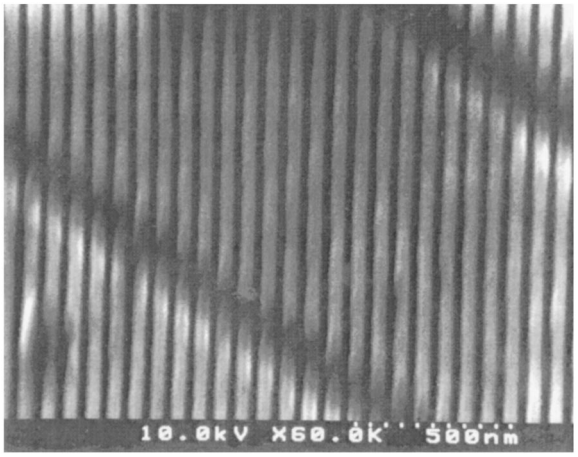

FIG. 4. Top view of 35 nm lines and spaces etched in silicon.

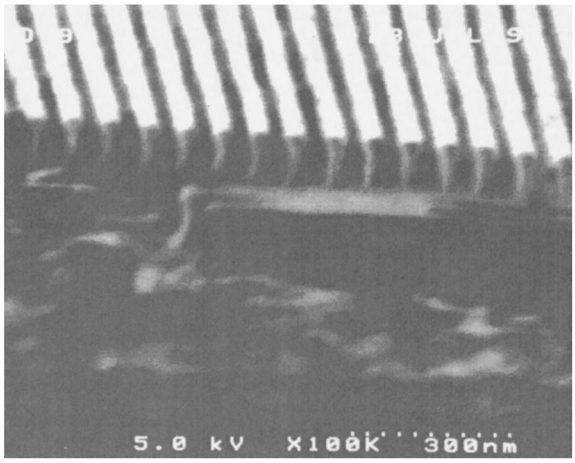

FIG. 5. Tungsten ICP etch profile with SF_6 at $-20\,^{\circ}C$ (30 nm lines and spaces). Some etching of underlying silicon has taken place, resulting in a rough surface beneath the tungsten.

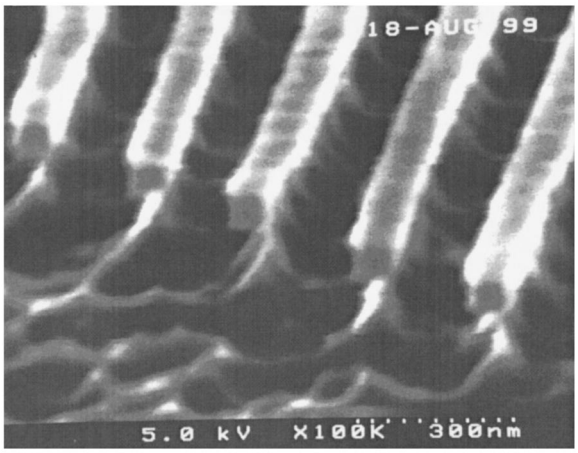

FIG. 6. Tungsten ICP etch profile with SF_6/O_2 at $-20\,^{\circ}C$. Some etching of underlying silicon has taken place, resulting in a rough surface beneath the tungsten.

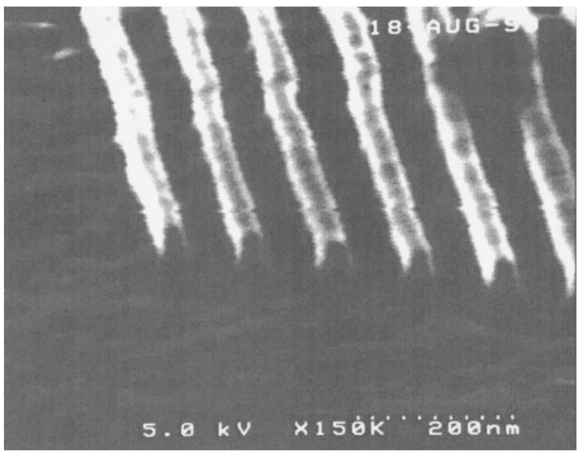

FIG. 7. Tungsten ICP etch profile with SF_6 at $-50\,^{\circ}C$.

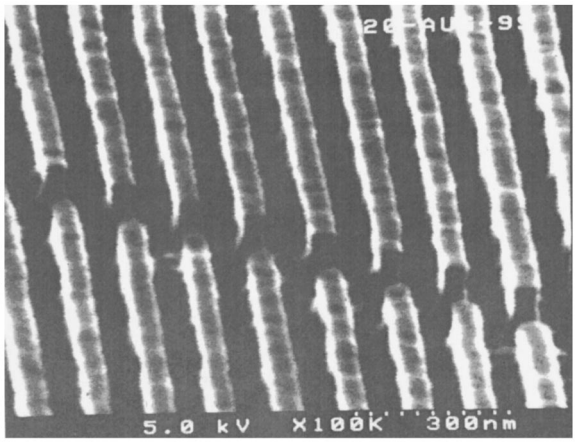

FIG. 8. Tungsten ICP etch profile with SF_6 at $-40\,^{\circ}C$.

led to rapid etching of the tungsten, which was too fast for control over the etch depths required, hence ICP power was reduced.

Low pressure operation was selected to obtain optimum anisotropy and best pattern definition in narrow linewidths.

A comparison of etch profiles at a variety of temperatures with and without O_2 addition is given in Figs. 5, 6, 7, and 8.

At $-20\,^{\circ}C$ with no O_2 addition the 30 nm lines exhibited a clear ''hourglass'' profile, indicating insufficient sidewall passivation (Fig. 5). When adding $10\%O_2$ to the $-20\,^{\circ}C$ process there was an improvement in etched profile (Fig. 6).

When operating at $-50\,^{\circ}C$ with no O_2 addition, the etch profile appeared to have a slight positive slope, indicating excess sidewall pasivation (Fig. 7).

At a temperature of $-40\,^{\circ}C$ (either with or without addition of $10\%O_2$) the profiles are vertical (Figs. 8 and 9).

This process gave a tungsten etch rate of 600 Å/min, with selectivity to Cr of $>20{:}1$. The low substrate temperature, held uniform across the wafer, is essential for producing the

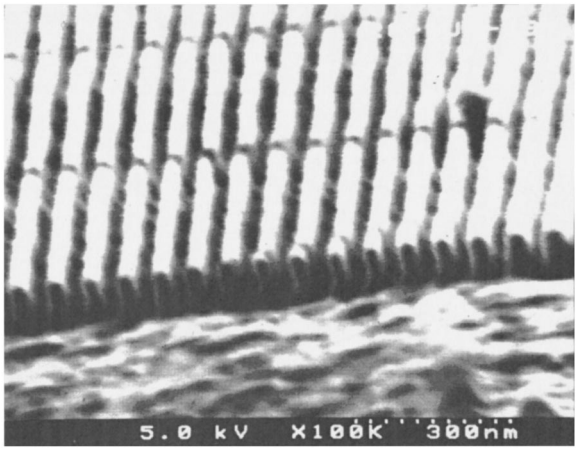

FIG. 9. Tungsten ICP etch profile with SF_6/O_2 at $-40\,^{\circ}C$ (30 nm lines and spaces).

highly anisotropic profile shown in Figs. 8 and 9. With this process, 30 nm lines with a 3:1 aspect ratio were transferred into tungsten.

VI. SUMMARY AND CONCLUSIONS

Etching of high resolution gratings in silicon and tungsten has been successfully demonstrated through the use of ICP dry etching with accurate substrate temperature control. Silicon ICP etching was carried out using a HBr process with a LTO mask layer. Highly anisotropic etch results were achieved at an etch rate of 800 Å/min and a selectivity of $>$10:1 to LTO for an etch depth of 200 nm.

Tungsten etching was carried out using an SF_6/O_2 based ICP process at low substrate temperature. The optimum etch conditions for anisotropic results used 10% added O_2 and a substrate temperature of $-40\,^{\circ}C$. An etch rate of 600 Å/min and a selectivity to Cr of $>$20:1 were achieved for an etch depth of 100 nm.

ICP etching with precise substrate temperature control as demonstrated in this article is a novel technique for pattern transfer of finely packed 30 nm features and below.

ACKNOWLEDGMENTS

The authors wish to thank Ted Blatchford and Geoff Thomas of Rutherford Appleton Laboratories for scanning electron microscopy examination of the wafers.

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