# Soldering to a single atomic layer

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The standard technique to make electrical contact to nanostructures is electron beam lithography. This method has several drawbacks including complexity, cost, and sample contamination. We present a simple technique to cleanly solder submicron sized, Ohmic contacts to nanostructures. To demonstrate, we contact graphene, a single atomic layer of carbon, and investigate low- and high-bias electronic transport. We set lower bounds on the current carrying capacity of graphene. A simple model allows us to obtain device characteristics such as mobility, minimum conductance, and contact resistance. © *2007 American Institute of Physics*. [DOI: 10.1063/1.2812571]

The conventional method of electrically contacting nanostructures is electron-beam lithography.[1] While having good resolution, the procedure is complex, expensive, and time consuming. Moreover, the polymer resists and solvents used in the process leave residues that contaminate the sample or device. As a result, often the major contribution to the device resistance is not from the sample itself but from the contacts.[2] Other lithography-free contacting techniques (such as shadow masks[3]) have been attempted, but they have their own drawbacks and have not been widely used. Here, we present an alternative method, effectively a miniaturization of soldering, which allows us to make submicron sized, Ohmic contacts to nanostructures of even single atom thickness. The technique is simple, inexpensive, rapid, and entirely avoids sample contamination.

Figure 1 shows the main components of the nanosoldering setup: an optical microscope, a micromanipulator, and a heated sample holder. The sample to be contacted is placed on the holder along with a small bead of indium. The temperature of the holder is then raised to 170 °C, roughly 20 °C above indium's melting point. The room-temperature tungsten tip is inserted into the molten bead using the microscope and micromanipulator *XYZ* translation stages, and a spike of solder is slowly pulled out. Submicron spike tips [Fig. 1, scanning electron microscopy (SEM) image] are possible with careful adjustment of the temperature and pullout rate. The sample and spike tip are then successively positioned and aligned under the microscope using both *XYZ* stages. The microscope stage is then quickly raised, fusing the solder spike onto the sample as it comes into contact. Once all contacts are made, the sample heater is turned off and the contacts solidify to produce a device (Fig. 1, optical image).

Several low-temperature melting point alloys of indium and tin (Indalloy 1E, 4, 121, 182, 290) have also been used to make contacts. Indium is desirable because of its good adhesion to numerous surfaces, including silicon oxide. Flux and flux-bearing solders are avoided so as to keep the sample free from residues. In fact, flux as well as inert or forming gases which would normally be required to make a good bond, are unnecessary with this technique. Since the tungsten tip which draws out the solder spike is at room temperature, oxidation of the solder spike is minimal.[4] Sample oxidation is also negligible for carbon nanostructures, since oxidation in air is significant only above 350 °C,[5–7] and for these materials, only solders with eutectic or melting points in the range of 118–280 °C are used. Ultimately, once the procedure is fine tuned, the nanosolder contacts are extremely reliable.

Using this technique, we contacted graphene,[8] single sheets of graphite which are extracted by micromechanical exfoliation.[9,10] This material has garnered much attention due to interesting physics and promise for applications.[11–14] Single sheet samples are identified optically by contrast analysis[15] and confirmed by the existence of a sole peak near 2700 $cm^{-1}$ in their Raman spectrum.[16] Once a suitable sample is isolated, contacts can be soldered to produce a working device within minutes. A typical optical image of a nanosolder contacted graphene device with two terminals is shown in Fig. 1. Samples are usually 10–20 $\mu$m in size, with contact separations typically several microns.

Figure 2 shows the source-drain current $I_{sd}$ of a nanosoldered graphene device measured as a function of applied voltage $V_{sd}$ in the range of ±10 V at room temperature in ambient conditions. The *IV* characteristic is linear even up to such high source-drain voltages. The resistance of the device, from the linear fit (dashed line), is 5.7 kΩ. The inset, an *IV* trace taken in the range $V_{sd}=\pm 10$ mV, gives a low-bias resistance of 6.0 kΩ, differing by 5% despite the 1000 times

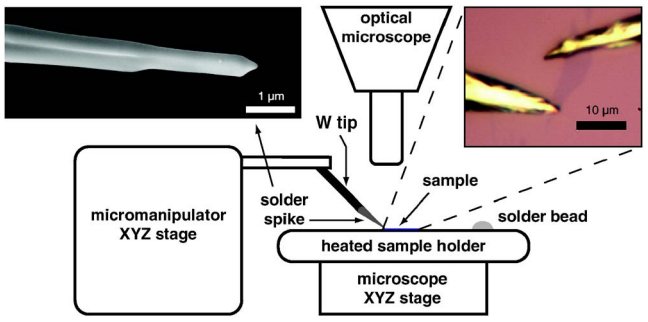


FIG. 1. (Color online) Schematic of the nanosoldering setup, consisting of an optical microscope, micromanipulator, and sample heater, used to contact graphene and other nanostructures. Upper left: scanning electron microscope image of an indium solder spike ending in a 50 nm radius tip (scale bar, 1 $\mu$m). Upper right: optical microscope image of a contacted graphene device (scale bar, 10 $\mu$m).

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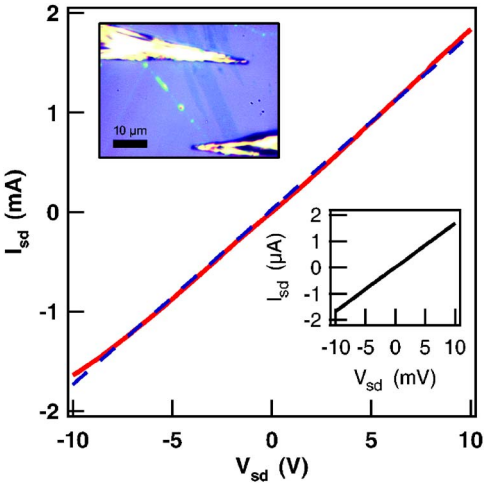


FIG. 2. (Color online) Source-drain current-voltage characteristic, with source-drain voltage $V_{sd}$ in the range of ±10 V, of the solder contacted graphene device shown in the inset, optical image (scale bar 10 $\mu$m, image contrast enhanced). Dashed line is linear fit to resistance 5.7 kΩ. Inset plot is low-bias *I-V* curve of same device, with a resistance of 6.0 kΩ. The back-gate voltage $V_{bg}$=0 V.

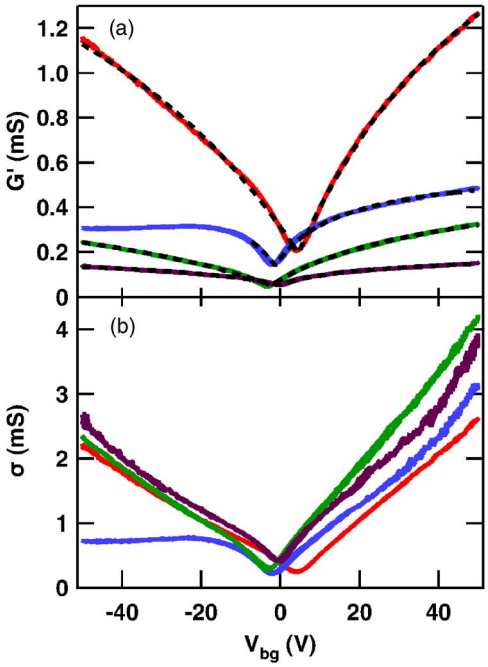


FIG. 3. (Color online) (a) Two-terminal conductance $G'$ of four solder-contacted graphene devices measured as a function of back-gate voltage $V_{bg}$. The dashed black lines are fits to the data with a Drude model modified to account for the electric field effect and the contact resistance. (b) Intrinsic sheet conductivities for the same devices obtained by subtracting the contact resistance as determined from the fits and accounting for the device aspect ratios. Gate voltage is swept both ways, showing negligible hysteresis.

smaller range in $V_{sd}$. Taking the device geometry into account, a lower bound on the current carrying capacity of single layer graphene in air on a silicon oxide substrate can be placed at 390 A/m (where per meter refers to the sheet width) or 120 MA/cm$^2$ bulk assuming a sheet thickness of 3.35 Å, the graphite interlayer spacing. This bulk current carrying capacity is more than 1000 times that of a superconductor.[17] Since our value is a lower bound, it is quite probable that the actual limit is comparable to that of multiwall carbon nanotubes,[18] roughly $10^9$ A/cm$^2$. In vacuum ($10^{-5}$ mbar), we have observed current densities in graphene as high as 500 A/m without device failure. Assuming uniform power dissipation, the power density of the device in Fig. 2 is 16 kW/cm$^2$, more than two orders of magnitude larger than the present processor heat flux.[19] With such high current carrying capacities and power densities, graphene electronics as envisaged, for example, by Berger *et al.*,[14] are expected to operate reliably at far higher power levels than possible for conventional Si-based devices.

Figure 3(a) shows the two-terminal conductances $G'$ of four soldered graphene devices as a function of back-gate voltage $V_{bg}$ at room-temperature in vacuum. All graphene samples, identically prepared and solder contacted are remarkable in that their Dirac points $V_D$—the location of the conduction minimum—are within 5 V of $V_{bg}$=0 V without any annealing or processing. This is in contrast with the literature of electron-beam lithographed devices,[20] where $V_D$ in the tens of volts is common. The clean, solder-contacted samples, without lithography residues to charge the sample and shift the Dirac point away from zero, are at least neutral, if not undoped. This is an important indication of how processing parameters influence the device characteristics.

Although these are two terminal measurements, we can nevertheless estimate the effective, or device, mobility, the minimum conductivity, and the contact resistance with a simple model. We relate the Drude equation for conductivity, $\sigma=en\mu$, with $n$ as the carrier density and $\mu$ as the mobility, to the conductance using $\sigma=GL/W$. The experimentally measured conductance $G'$ includes the contact resistance $R_c$ via $1/G'=R_c+1/G$. For graphene in a standard transistor geometry, the carrier density depends on the back-gate voltage as $n=c'|V_{bg}-V_D|/e$, where the specific capacitance $c'$ for a 300 nm silicon oxide gate thickness is 115 aF/$\mu$m$^2$. Finally, we add a phenomenological parameter $\sigma_D$ to account for the nonzero minimum conductance and allow differing electron and hole mobilities $\mu_e$ and $\mu_h$ to obtain

$$\frac{1}{G'} = R_c + \frac{L/W}{c'\mu_{e,h}|V_{bg} - V_D| + \sigma_D}, \tag{1}$$

using $\mu_e$ for back-gate voltage $V_{bg} \geqslant V_D$ and $\mu_h$ in the range $V_{bg} < V_D$. The aspect ratio, $L/W$, is determined from optical images of the devices. In general, this model will overestimate the contact resistance as any intrinsic sublinearity in the conductance-gate voltage curves[21] will contribute to $R_c$. While the data can be fitted to more fundamental theories,[22] the simple model suffices here to characterize the graphene devices.

Figure 3(b) plots the intrinsic device conductivity, $\sigma=L/W(1/G'-R_c)$, as a function of applied back-gate voltage $V_{bg}$, where the contact resistance $R_c$ is extracted from the fits [Fig. 3(a), dashed black lines]. The conductivity curves are relatively linear for almost all the devices, indicating the fit is good. Note that it is clear from the plots that the mobilities (slopes of the curves) and minimal conductivities are roughly the same for all devices. The electron mobilities range from 4500 to 6200 cm$^2$/V s and hole mobilities range from 3000 to 3600 cm$^2$/V s, show much less variation than, in electron-beam lithography defined devices.[20] The minimal conductivities are 210, 230, 300, and 440 $\mu$S. The contact resistance per lead over nine devices varied from 190 to 1700 Ω, with a mean of 680 Ω and a standard deviation of 450 Ω, comparable to the best electron-lithography fabricated devices.[23]

The solder contact method can also be used to contact nanotubes and nanowires. We have used SEM to locate multiwall carbon nanotubes relative to predefined optically visible markers. The soldering technique, as described above, can then be used by positioning the leads relative to the markers. However, a better method would be to use a piezomicromanipulator inside the SEM itself, along with a heated sample stage, and solder the contacts *in situ*. Other applications of the solder technique are wirebonding and shadow mask alignment. To wirebond devices which already have leads, fine wire is placed near the leads and then a solder spike is deposited, with the sample stage hot, over both lead and wire. When the heater is turned off, the solidified spike fixes the wire to the substrate and provides electrical contact to the lead. The wirebonding and sample soldering can also be performed in a single step, with the solder spike both contacting the sample and fixing the wire. To align shadow masks, a similar process is used. The mask is placed on top of the substrate, over the sample, and soldered at the corners. The micromanipulator is then used to push the mask into alignment, and the heater is turned off to fix the mask.

Solder contacts are a simple, efficient means of producing functional nanostructure devices based on graphene, nanotubes, or other materials. Not only the contacts are Ohmic, but also the resultant devices are clean and the device characteristics are consistent. The contacts, capable of sustaining large currents without failure, allow for investigation of high-bias electronic transport properties.

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